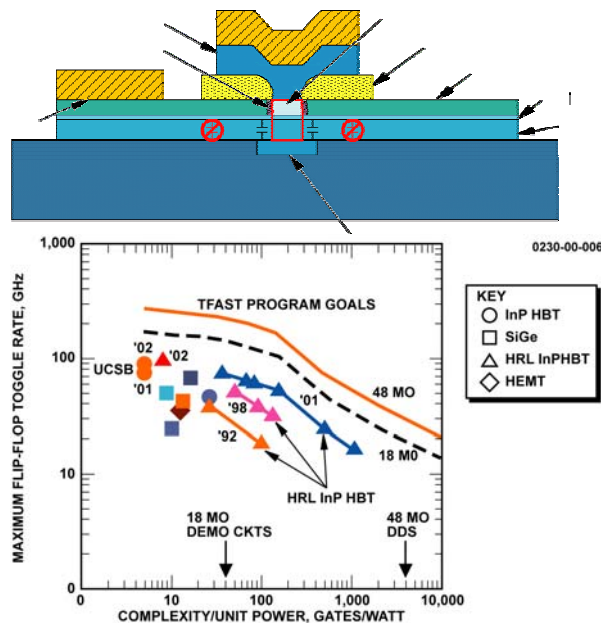


## Graphic of Technology



## Goals, Objectives and Main Technical Approach

Demonstrate 250 nm Emitter Transistors  
 $f_t = 350$  GHz,  $f_{max} = 400$  GHz (Phase IA)  
 150 GHz Static Flip-flop (Phase IA)  
 30 mW power per flip-flop at speed  
 20,000 HBT Integration level (Phase II)  
 Minimize access resistances and parallel capacitance to an optimized intrinsic InP HBT transistor.

## Major Technical Accomplishments (since start of contract)

Demonstration of ion implantation with low sheet resistance ( $14 \Omega/\text{square}$ ) and subsequent MBE regrowth of device grade HBT material on large area substrate.

## Major Work Remaining to Completion of Contract

Demonstration of low parasitic HBT and static divider at 150 GHz.

## Major Impact of Technology & Technology Transition Plan

3x clock rate, 10x power reduction and 10x integration level for high performance integrated circuits to enable advanced DoD system concepts.

Direct digital synthesis of X-band signals using conventional DDS architecture. Ability to realize digital synthesis of 40 GHz signals and above using  $\Delta\Sigma$  architecture. (5x the current DDS)